**Op-Code Information**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Op-Code Set | Instr | Op-Code | Remaining Bits | |
|  | | | | |
| Halt | Halt | 00 | XXXXXX | |
| Branches | Bra | 01 | 000001 | |
| Beq | 01 | 000010 | |
| Bgt | 01 | 000100 | |
| Bnz | 01 | 001000 | |
| Multi-Purpose | Add | 10 | 000 | 000 |
| Adds | 10 | 000 | 001 |
| Inc | 10 | 001 | 000 |
| Dec | 10 | 001 | 001 |
| Wdt | 10 | 010 | 000 |
| InitR1 | 10 | 100 | 000 |
| InitR2 | 10 | 100 | 001 |
| InitR3 | 10 | 100 | 010 |
| InitR4 | 10 | 100 | 011 |
| Load & Store | Ld1 | 11 | 0 | 00001 |
| Ld2 | 11 | 0 | 00010 |
| Ld3 | 11 | 0 | 00011 |
| Ld4 | 11 | 0 | 00100 |
| Ld5 | 11 | 0 | 00101 |
| Ld6 | 11 | 0 | 00110 |
| St1 | 11 | 1 | 00001 |
| St2 | 11 | 1 | 00010 |
| St3 | 11 | 1 | 00011 |
| St4 | 11 | 1 | 00100 |
| St5 | 11 | 1 | 00101 |

**Register/Memory Information**

* 4 8-bit Registers
* 64 Byte Data Memory
  + 6-bit addressing

**Instruction Descriptions**

|  |  |
| --- | --- |
| Bra | PC -9 |
| Beq | If R1 = 63, PC +1 |
| Bgt | If R4 > R3, PC +3 |
| Bnz | If R1 is not 0, PC -3 |
| Add | Adds R2 + [R4 + R3], store to R3 |
| Adds | Takes overflow latch and store to R4 |
| Inc | Increments R1 |
| Dec | Decrements R1 |
| Wdt | Calculates bit width of R2 and store to R3 |
| InitR1 | Load R1 with 0 |
| InitR2 | Load R2 with 0 |
| InitR3 | Load R3 with 0 |
| InitR4 | Load R4 with 0 |
| Ld1 | Load R1 with number at memory location 0 |
| Ld2 | Load R2 with number at memory location 0 |
| Ld3 | Load R3 with number at memory location 0 |
| Ld4 | Load R1 with binary number 31 |
| Ld5 | Load R2 with number at memory location held in R1 |
| Ld6 | Load R4 with number in R3 **OR** Load R4 with number at mem. loc. 3 |
| St1 | Store R4 at memory location 1 |
| St2 | Store R3 at memory location 2 |
| St3 | Store R3 at memory location 3 |
| St4 | Store R2 at memory location 4 |
| St5 | Store R1 at memory location 5 |